PG2402

48 Gb/s Pattern Generator, Dual 24 Gb/s Channel

The Optilab PG2402 is a Dual 24 Gb/s Pattern Generator (PG) combined, for 48 Gb/s. This high performance pattern generator unit provides up to 24 Gb/s eye diagram generation for Bit Error Rate Testing (BERT). The user selectable reference clock allows testing BER at a specific data rate with external clock input or at a pre-defined data rate using the internal clock. A high speed synchronized clock at half or full data rate is available for eye pattern monitoring or RZ pulse generation. An intuitive GUI, Optilab Teraport, is provided with the BERT system for easy operation. Contact Optilab for more information.

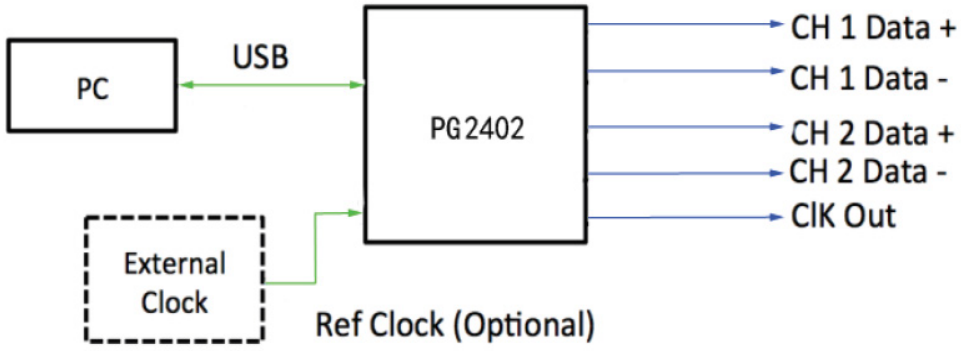
Features

- Data Rate from 2x20 to 2x24 Gbps
- PRBS of 2^7-1 or 2^{31}-1
- Integrated DQPSK Precoder
- Error injection function
- Teraport GUI software included
- Differential output adjustable to 1 volt
- Eye Crossing Adjustment

Applications

- Photonics module testing
- Electrical eye diagram to 24 Gb/s x2
- 43 Gbps DQPSK link
- 100 Gbps DP-QPSK testing

Functional Diagram



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OPTIONS

PG2402-XX

XX
Clock:
11: External Clock
Adjustment
20: 20 Gb/s fixed
24: 24 Gb/s fixed

TECHNICAL INFO

For technical info and support:

sales@optilab.com

www.optilab.com

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Optilab Advantage

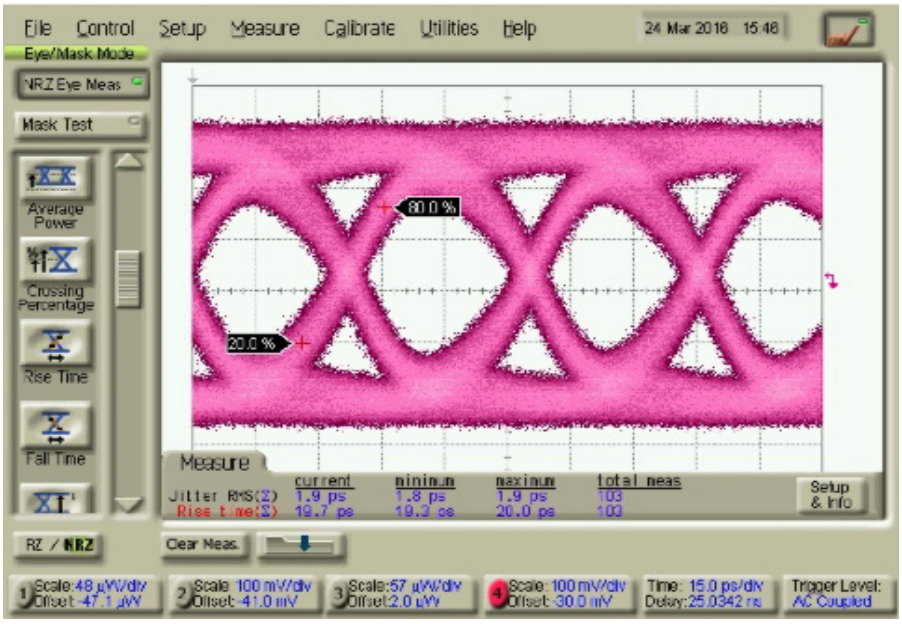
- Innovation
- Performance
- Quality
- Customization
- Warranty

Data Output Specifications	
Data Pattern	128 bit Fixed pattern PRBS (2^7-1 or 2^31-1)
Data Output Type	DC Coupled, Differential
Output Data Rate	20 Gb/s min., 24 Gb/s max.
Output Data Amplitude	0.1 Vpp min., 1 Vpp max.
Differential Output Impedance	100 Ω typ.
Data Output RMS Jitter	1.9 ps typ.
Rise/Fall time (20% to 80%)	20 ps typ.
Electrical Connectors	2.92 mm Female (K or SMA compatible)

Clock Input Specifications	
Ref Clock Input Frequency	622.5 MHz min., 750 MHz max.
Ref Clock Input Amplitude	-5 dBm min., 0 dBm typ., 3 dBm max
HS Clock Output Frequency	10 GHz (half), 12 GHz (full) min.; 20 GHz (half), 24 GHz (full) max.
HS Clock Phase adjustment Range	0.9 UI min., 1.0 UI typ.
Clock Connectors	SMA female

Mechanical Specifications	
Operating Temperature (standard)	0 °C to +50 °C
Storage Temperature	-40 °C to +70 °C
Power Supply Requirements	80 - 240 V, 43 - 63 Hz AC.
Power Consumption	60 W max.
Dimensions	476.6 mm x 482.6 mm x 44.5 mm

Eye Diagram Example



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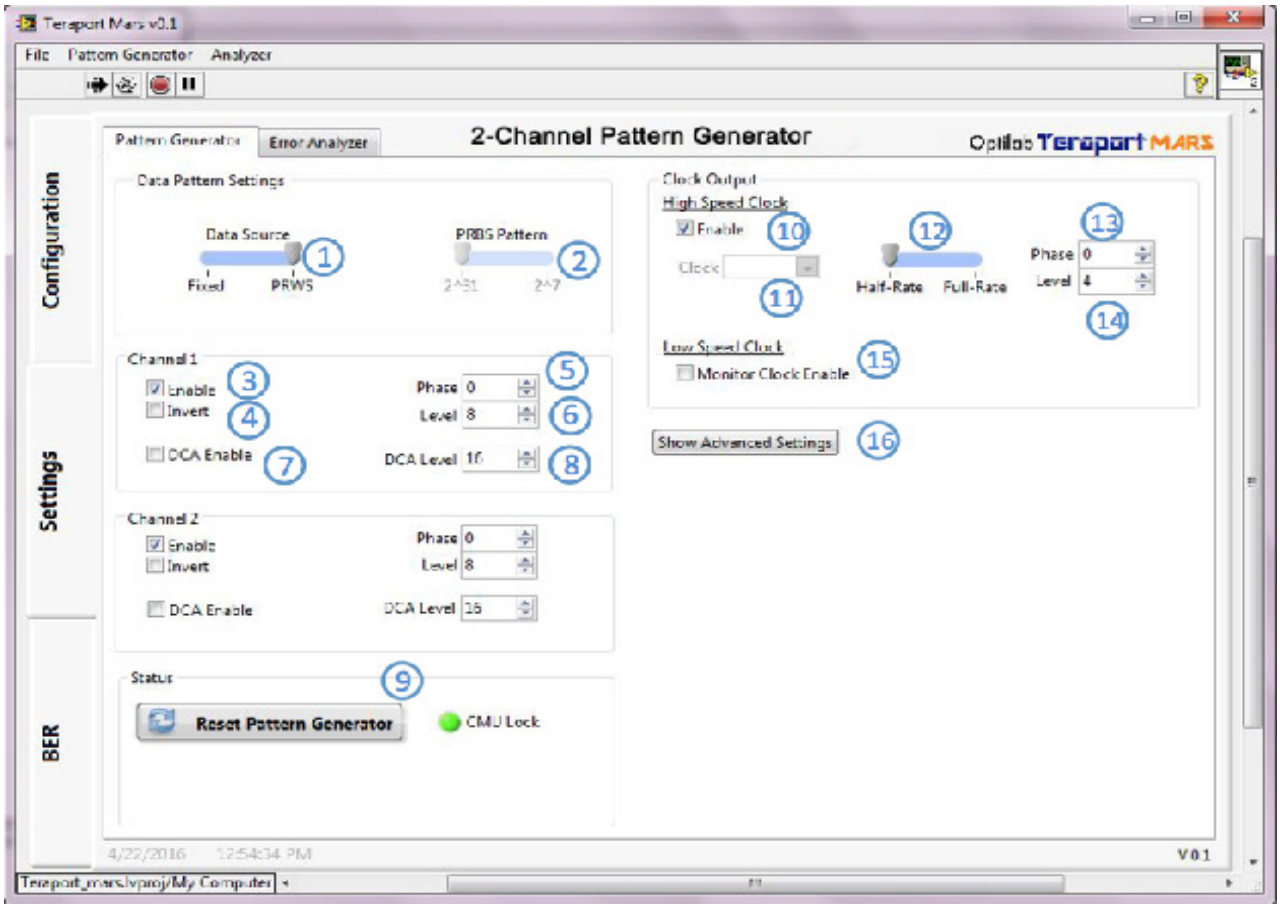
Teraport Interface



No.	Function	Description
①	Data Source	Fixed or PRBS pattern
②	PRBS Pattern	2^7-1 or 2^31-1
③	Enable	Enable channel
④	Invert	Invert data pattern
⑤	Phase	Phase adjust
⑥	Level	Output voltage level
⑦	DCA Enable	Turn on data crossing adjustment
⑧	DCA Level	Data crossing adjustment level
⑨	Reset Pattern Generator	Reset operation
⑩	Enable	Turn on high speed clock output
⑪	Clock	Select clock
⑫	Half Rate, Full Rate	Select half or full rate
⑬	Phase	Phase adjustment
⑭	Level	Clock output level adjustment
⑮	Monitor Clock Enable	Turn on low speed clock
⑯	Show Advanced Setting	Additional control function

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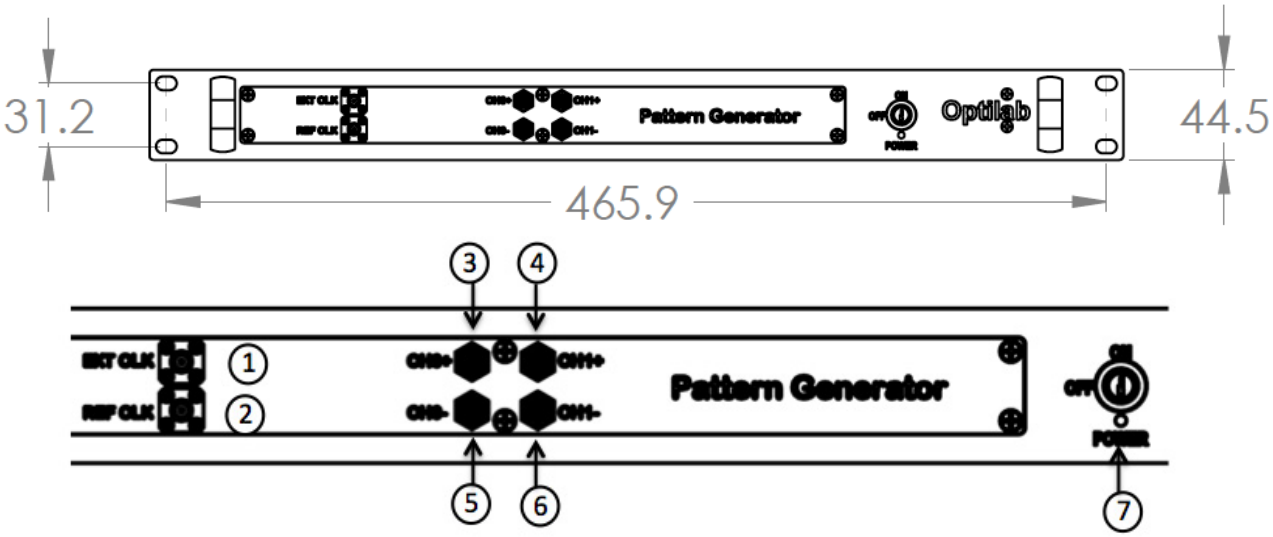
Mechanical Drawing



No.	Function	Description
1	External Clock	External clock input port
2	Reference Clock	High speed clock output port
3	CH 1+	Channel 1,data+
4	CH 2+	Channel 2,data+
5	CH 1-	Channel 1,data-
6	CH 2-	Channel 2,data-
7	Power	Turn on /off

Available Clock Rate Option

External	Adjustment from 20 Gb/s to 24 Gb/s
20G	Builtin clock for 20 Gb/s output
24G	Builtin clock for 24 Gb/s output
Custom	Any fixed clock from 622.5MHz to 750 MHz